

Please amend the claims as follows:

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25. (Six times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:  
a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;  
at least one p-well and at least one n-well on said substrate first surface;  
at least one activated, annealed p-type area within said at least one n-well and at least one activated, annealed n-type area within said at least one p-well; and  
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

26. (Previously amended) The structure of claim 25 further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

31. (Previously amended) The structure of claim 25, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon nitride.

32. (Previously amended) The structure of claim 25, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.

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33. (Four times amended) An intermediate structure in the formation of an isolation structure for a semiconductor device, comprising:  
a semiconductor substrate free of field oxide structures and having a first surface and a second surface, said first surface opposing said second surface;

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at least one p-well and at least one n-well on said substrate first surface;  
at least one activated, annealed doped area within at least one of said at least one n-well and said  
at least one p-well; and  
a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface  
and said second surface of said semiconductor substrate, said substantially dopant-free,  
uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

6 34. The structure of claim 33 further comprising a layer of oxide  
between said substrate first surface and said substantially dopant-free, uninterrupted diffusion  
barrier layer.

7 37. The structure of claim 33, wherein said substantially dopant-free,  
uninterrupted diffusion barrier layer comprises one of the group consisting of silicon nitride and  
silicon oxynitride.

8 38. (Amended) The structure of claim 33, wherein said at least one activated, annealed  
doped area comprises an impurity selected from the group consisting of an n-type impurity and a  
p-type impurity.

39. (Four times amended) An intermediate structure in the formation of an isolation  
structure for a semiconductor device, comprising:  
a semiconductor substrate free of field oxide structures and having a first surface and a second  
surface, said first surface opposing said second surface;  
at least one activated, annealed first doped area on said substrate first surface;  
at least one activated, annealed second, differently doped area within said at least one first doped  
area; and

53 [ a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface of said semiconductor substrate, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

10/ 40. The structure of claim 39<sup>9</sup> further comprising a layer of oxide between said substrate first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

I' 43. The structure of claim 39<sup>9</sup>, wherein said substantially dopant-free, uninterrupted diffusion barrier layer comprises one of the group consisting of silicon nitride and silicon oxynitride.

12/ 44. (Amended) The structure of claim 39<sup>9</sup>, wherein said at least one activated, annealed first doped area comprises a p-type impurity and said at least one activated, annealed second, differently doped area comprises an n-type impurity.

13/ 45. (Amended) The structure of claim 39<sup>9</sup>, wherein said at least one activated, annealed first doped area comprises an n-type impurity and said at least one activated, annealed second, differently doped area comprises a p-type impurity.

Part 54 46. (Twice Amended) An intermediate structure useful in the formation of electrical device isolation structures, comprising:  
a semiconductor substrate that is free of field oxide structures and includes a first surface and a second surface, said first surface opposing said second surface;  
at least one p-well and at least one n-well defined on said first surface of said substrate;  
at least one activated, annealed p-type area defined within said at least one n-well and at least one activated, annealed n-type area defined within said at least one p-well; and

54 [ a substantially dopant-free, uninterrupted diffusion barrier layer extending over said first surface and said second surface, said substantially dopant-free, uninterrupted diffusion barrier layer encapsulating said semiconductor substrate.

15 47. (Amended) The structure of claim 46 further comprising a layer of oxide between said first surface and said substantially dopant-free, uninterrupted diffusion barrier layer.

I' 16 48. (Amended) The structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon nitride.

17 49. (Amended) The structure of claim 46, wherein said substantially dopant-free, uninterrupted diffusion barrier layer is silicon oxynitride.